Program Name : **Electronics Engineering Programme Group**

Program Code : **DE/EJ/ET/EN/EX/EQ**

Semester : **Sixth**

Course Title : **VLSI with VHDL**

Course Code : **22062**

1. RATIONALE

In the present scenario of electronics technology, CMOS is a vital important and basic need in the design/development of almost all products in the range from consumer to industrial and telecommunication engineering area. Functional capabilities of this technology leads to advanced Very Large Scale Integration, large density of components, high speed of operation, less area with less power dissipation. Therefore imparting knowledge of VLSI and its tools is need of today. After completion of this course, students will be able to develop applications in the area of digital electronics using VLSI design tools.

2. COMPETENCY

The aim of this course is to help the student to attain the following industry identified competency through various teaching learning experiences:

- **Maintain VLSI based electronic circuits .**

3. COURSE OUTCOMES (COs)

The theory, practical experiences and relevant soft skills associated with this course are to be taught and implemented, so that the student demonstrates the following industry oriented COs associated with the above mentioned competency:

a. Develop design flow for the given application using VLSI tools.
b. Interpret CMOS technology circuits with their specifications.
c. Use relevant VHDL model for given application.
d. Debug VHDL program for the given application.
e. Maintain FPGA based circuits

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme			Credit (L+T+P)	Examination Scheme												
				Theory							Practical					
L	T	P		Paper Hrs.	ESE		PA		Total		ESE		PA		Total	
					Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
2	-	2	4	--	--	--	--	--	--	--	25#	10	25~	10	50	20

(*): Under the theory PA, Out of 30 marks, 10 marks are for micro-project assessment to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for the assessment of the cognitive domain UOs required for the attainment of the COs.

Legends: ***L****-Lecture;* ***T*** *– Tutorial/Teacher Guided Theory Practice;* ***P*** *- Practical;* ***C*** *– Credit,* ***ESE*** *- End Semester Examination;* ***PA*** *- Progressive Assessment.*

5. COURSE MAP (with sample COs, PrOs, UOs, ADOs and topics)

This course map illustrates an overview of the flow and linkages of the topics at various levels of outcomes (details in subsequent sections) to be attained by the student by the end of the course, in all domains of learning in terms of the industry/employer identified competency depicted at the centre of this map.

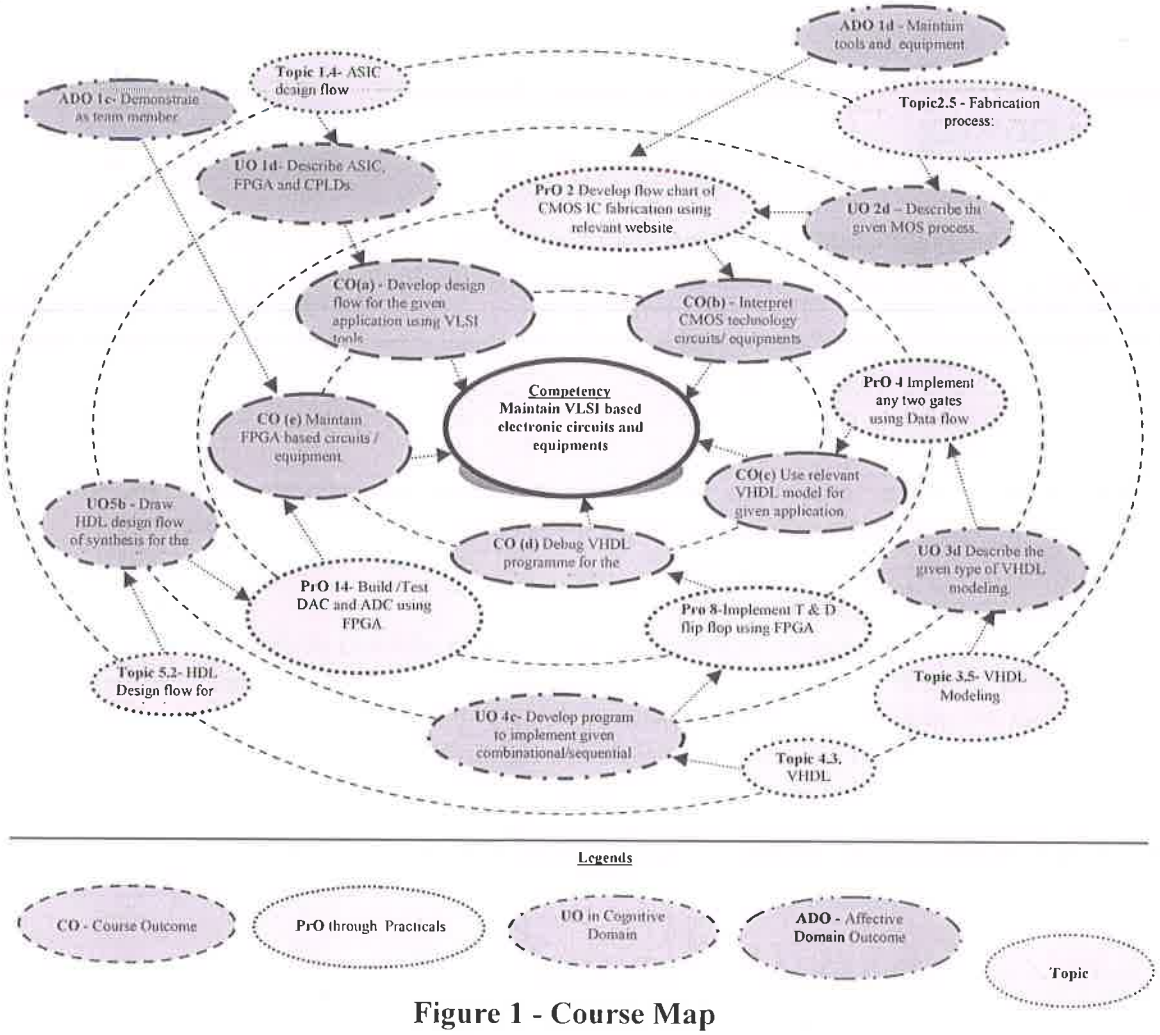

Figure 1 - Course Map

6. SUGGESTED PRACTICALS/ EXERCISES

The practicals in this section are PrOs (i.e. sub-components of the COs) to be developed and assessed in the student for the attainment of the competency.

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Identify internal block and pin configuration of FPGA & CPLD using datasheet.	I	02*
2	Develop flow chart of CMOS IC fabrication using relevant website.	II	02*
3	Install EDA tool (VHDL) for VLSI application.	III	02*
4	Implement any two gates using Data flow and Behavioral model.	IV	02*
5	Implement Half /full adder / subtractor using FPGA	IV	02

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
6	Implement 8:1 multiplexer using FPGA	IV	02
7	Implement 1:8 Demultiplexer using FPGA	IV	02
8	Implement T& D-flip-flop using FPGA	IV	02
9	Implement 2:4 Decoder using FPGA	IV	02
10	Implement 8:3 Encoder using FPGA	IV	02
11	Implement up-counter using FPGA	IV	02
12	Implement synchronous counter using FPGA	IV	02
13	Implement binary to gray code converter using FPGA.	IV	02
14	Build /Test DAC using FPGA.	V	02*
15	Implement Stepper motor controller using FPGA.	V	02
16	Implement four Bit ALU or sequence generator using FPGA.	V	02*
	Total		**32**

Note

*i. A suggestive list of **PrOs** is given in the above table. More such PrOs can be added to attain the COs and competency. A judicial mix of minimum 12 or more practical need to be performed, out of which, the practicals marked as '*' are compulsory, so that the student reaches the 'Precision Level' of Dave's 'Psychomotor Domain Taxonomy' as generally required by the industry.*

ii. The 'Process' and 'Product' related skills associated with each PrO is to be assessed according to a suggested sample given below:

S. No.	Performance Indicators	Weightage in %
a.	Preparation of experimental set up	20
b.	Setting and operation	20
c.	Safety measures	10
d.	Observations and Recording	10
e.	Interpretation of result and conclusion	20
f.	Answer to sample questions	10
g.	Submission of report in time	10
	Total	**100**

The above PrOs also comprise of the following social skills/attitudes which are Affective Domain Outcomes (ADOs) that are best developed through the laboratory/field based experiences:

a. Follow safety practices.
b. Practice good housekeeping.
c. Demonstrate working as a leader/a team member.
d. Maintain tools and equipment.
e. Follow ethical practices.

The ADOs are not specific to any one PrO, but are embedded in many PrOs. Hence, the acquisition of the ADOs takes place gradually in the student when s/he undertakes a series of practical experiences over a period of time. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

- 'Valuing Level' in 1st year
- 'Organizing Level' in 2nd year
- 'Characterizing Level' in 3rd year.

7. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

The major equipment with broad specification mentioned here will usher in uniformity in conduct of experiments, as well as aid to procure equipment by authorities concerned.

S. No.	Equipment Name with Broad Specifications	PrO. S. No.
1	Personal Computer with latest configuration.	All
2	FPGA trainer kit with accessories.	10-15
3	VLSI trainer kit along with peripherals such as switches, keyboard, LEDs, seven segment display.	1-15
4	VLSI trainer kit along with DAC, ADC trainer kit.	1-15
5	VLSI trainer kit along with stepper motor.	1-15
6	JTAG cable, DMM, Bread Board.	1-16
7	Xilinx/Altera or equivalent EDA tool.	13

8. UNDERPINNING THEORY COMPONENTS

The following topics/subtopics should be taught and assessed in order to develop UOs in cognitive domain for achieving the COs to attain the identified competency.

Unit	Unit Outcomes (UOs) (in cognitive domain)	Topics and Sub-topics
Unit – I Advanced Digital Design and ASIC, FPGA, CPLD.	1a. Differentiate between asynchronous and synchronous logic circuit for the given parameters. 1b. Develop the state diagram, state table for the given sequential logic. 1c. Develop model of Moore and Mealy machine of the given Contents. 1d. Describe the given ASIC, FPGA and CPLDs.	1.1 Review of Sequential Logic : Asynchronous and Synchronous, Metastability, Noise margins, Power Fan-out, Skew (Definitions only) 1.2 Moore and Mealy Models, state machine notation, 1.3 Examples on Moore and mealy: counter, sequence detector only 1.4 ASIC design flow 1.5 CPLD - Details of internal block diagram 1.6 FPGA - architecture, details of internal block diagram

Unit	Unit Outcomes (UOs) (in cognitive domain)	Topics and Sub-topics
Unit – II CMOS Technology concepts.	2a. Compare the performance of BJT and CMOS for the given parameters. 2b. Draw the simplified CMOS logic of the given gates. 2c. Explain CMOS inverter characteristics with relevant sketch. 2d. Describe the given MOS fabrication process.	2.1 Introduction of BJT and CMOS parameters 2.2 Basic gates using CMOS Inverter, NOR, NAND, MOS transistor switches, transmission gates, CMOS inverter characteristics. 2.3 Complex logic using CMOS 2.4 Estimation of resistance and capacitance layout. 2.5 Fabrication process: Overview of wafer processing, Oxidation, epitaxy, deposition, Ion–Implementation and diffusion, silicon gate process. 2.6 Basics of NMOS, PMOS and CMOS: nwell, pwell, twin tub process.
Unit– III Introduction to VHDL	3a. Describe Hardware description language, its components and programming syntax. 3b. Describe the given VHDL flow elements. 3c. Describe the use of given data type declaration in VHDL. 3d. Describe the given type of VHDL modeling.	3.1 Introduction to HDL: History of VHDL, Pro's and Con's of VHDL 3.2 VHDL Flow elements:-Entity, Architecture, configuration, package, library only definitions. 3.3 Data Types, operators, operations. 3.4 Signal, constant and variables (syntax and use). 3.5 VHDL Modeling: - Data flow, Behavioral, Structural.
Unit– IV VHDL Programming .	4a. Develop program using concurrent statements for the given application in VHDL. 4b. Develop program using sequential statements for the given application in VHDL. 4c. Develop program to implement the given combinational /sequential logic circuit using VHDL. 4d. Describe the test bench for the given application in VHDL.	4.1 Concurrent constructs (when, with). 4.2 Sequential Constructs (process, if, case, loop, assert, wait) 4.3 VHDL program to implement Flip Flop, Counter, shift register, MUX, DEMUX, ENCODER, DECODER, MOORE, MEALY machines . 4.4 Test bench and its applications.
Unit– V HDL Simulation and Synthesis.	5a. Describe VHDL simulation for the given application. 5b. Draw HDL design flow of synthesis for the given application. 5c. Describe use of efficient coding styles, optimizing expression, sharing of complex operator.	5.1 Event scheduling, sensitivity list, zero modeling, simulation cycle, comparison of software and hardware description language, delta delay. 5.2 HDL Design flow for synthesis 5.3 Efficient Coding Styles, Optimizing arithmetic expression, sharing of complex operator.

Note: To attain the COs and competency, above listed UOs need to be undertaken to achieve the 'Application Level' and above of Bloom's 'Cognitive Domain Taxonomy'.

9. SUGGESTED SPECIFICATION TABLE FOR QUESTION PAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Introduction to Advanced Digital Design Specific & and ASIC, FPGA, CPLD.	06	Not Applicable as no theory paper			
II	Introduction to CMOS Technology	04				
III	Introduction to VHDL	08				
IV	VHDL Programming.	08				
V	HDL Simulation and Synthesis.	06				
	Total	**32**				

Legends: *R=Remember, U=Understand, A=Apply and above (Bloom's Revised taxonomy)*
Note: This specification table provides general guidelines to assist student for their learning and to teachers to teach and assess students with respect to attainment of UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary from above table.

10. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of about 5 pages for each activity, also collect/record physical evidences for their (student's) portfolio which will be useful for their placement interviews:

a. Prepare the survey report on the VLSI based applications.
b. Compare technical specifications and applications of various types of memory, CPLDs, FPGA and Prepare report.
c. Refer basic requirement of PC configuration to install VLSI EDA tool.
d. Give seminar on any course relevant topic.
e. Conduct library / internet survey regarding different data sheet and manuals related CPLD, FPGA.
f. Prepare power point presentation on VLSI and their applications.
g. Undertake a market survey of companies profile related to VLSI and prepare report.
h. Search for video / animations / power point presentation on internet for complex topic related to the course and make a presentation.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various learning outcomes in this course:

a. Massive open online courses (***MOOCs***) may be used to teach various topics/sub topics.
b. ***'L' in item No. 4*** does not mean only the traditional lecture method, but different types of teaching methods and media that are to be employed to develop the outcomes.

c. About ***15-20% of the topics/sub-topics*** which is relatively simpler or descriptive in nature is to be given to the students for ***self-directed learning*** and assess the development of the COs through classroom presentations (see implementation guideline for details).
d. With respect to item No.10, teachers need to ensure to create opportunities and provisions for ***co-curricular activities***.
e. Guide student(s) in undertaking micro-projects.
f. PPTs/Animations may be used to explain the construction and working of electronic circuits.
g. Guide students for using data sheets / manuals.

12. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student assigned to him/her in the beginning of the semester. S/he ought to submit it by the end of the semester to develop the industry oriented COs. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course.

In the first four semesters, the micro-project could be group-based. However, in higher semesters, it should be individually undertaken to build up the skill and confidence in every student to become problem solver so that s/he contributes to the projects of the industry. A suggestive list is given here. Similar micro-projects could be added by the concerned faculty:

a. Prepare report of CMOS fabrication process.
b. Market Survey related to CMOS IC's and prepare report.
c. Develop four bit addition/subtraction.
d. Develop square wave generator of Frequency = 1Hz/ 100Hz.
e. A shopkeeper requires an alarm system when a customer enters into the shop through exits door. Develop a VLSI based system.
f. An indication for any maloperation in the given application is to be indicated by blinking of LEDs. Build a VLSI based system for the same.

Note: *Use FPGA kit and general purpose PCB for making micro projects*

13. SUGGESTED LEARNING RESOURCES

S. No.	Title of Book	Author	Publication
1	VHDL Basics to programming	Gaganpreet Kaur	Pearson Education India, 2011 ISBN 10: 8131732118 ISBN 13: 9788131732113
2	Digital Logic: Application and design	John M. Yarbrough	C.L Engineering, ISBN 10: 0314066756 ISBN 13: 978 0314066756

S. No.	Title of Book	Author	Publication
3	An engineering approach to digital design	Willian I. Fletcher	Prentice- Hall of India ISBN-13: 978-0132776998 ISBN-10: 0132776995
4	Principles of CMOS VLSI Design: A system perspective	Neil H. E. Weste Kamran Eshraghian	Pearson Education ISBN 10: 0201082225 / ISBN 13: 9780201082227
5	VHDL programming by example	Douglas Perry	Tata Mcgraw-hill; 4 edition (2002) ISBN-10: 0070499446 ISBN-13: 978-0070499447
6	Introduction to VLSI Design	Eugene D. Fabricus	McGraw Hill ISBN-13: 978-0070199484 ISBN-10: 0070199485
7	VLSI design and EDA tools	Sarkar & Sarkar	Scitech Publications (India) Pvt Ltd (December , 2013) ISBN-10: 8183714978 ISBN-13: 978-8183714976
8	Xilinx Manual	Xilinx	www.xilinx.com

14. SUGGESTED SOFTWARE/LEARNING WEBSITES

a. http://rti.etf.bg.ac.rs/rti/ri5rvl/tutorial/TUTORIAL/HTML/HOMEPG.HTM
b. http://iiith.vlab.co.in/?sub=21&brch=66&sim=531&cnt=1&lan=en-IN
c. http://www.vlsiencyclopedia.com/2012/12/loop-statement.html
d. https://books.google.co.in/books?id=RjdYEY8dJvwC&pg=SA3-PA47&lpg=SA3-PA47&dq=vlsi+next+statement&source=bl&ots=oS8dg9uQL6&sig=KHqaQMIgQ5CWkpC_c8Yfew_7h20&hl=en&sa=X&ved=0ahUKEwjx_5LQk5bLAhVRSo4KHcoGDDMQ6AEIPjAH#v=onepage&q=vlsi%20next%20statement&f=false
e. http://only-vlsi.blogspot.in/2007/12/vlsi-design-flow.html
f. http://www.vhdl.renerta.com/source/vhd00014.htm
g. http://www.csee.umbc.edu/portal/help/VHDL/summary.html
h. http://vlab.co.in/ba_labs_all.php?id=1